Fall 2003 – CSE 207 Digital Design Project #1

Background

The lowest bidder won the paving contract for UConn, and before they finished paving the streets, they ran out of money. Then they ran out of town. Now as students return for classes, the streets are partially paved and the buses cannot drop students in front of their buildings. Given the rain this summer, university planners are afraid that too many students will melt if they get wet, so allowing them to walk across campus is not an option. To solve the problem, university officials have decided to open the steam tunnels to students. These tunnels connect the four distant ends of the campus as shown in Figure 1.

The entry points to the tunnels are A, B, C, and D, which correspond to North, East, South, and West campus. The arrows show the paths of the tunnels that may be traversed. The longest legs are AC and BD. While they are great shortcuts across campus, they are also the smallest tunnels. University officials are concerned that too many students will try to fit in those tunnels at once and get stuck. To avoid this situation, they have decided to restrict access to those sections based on the time of day (peak or off-peak) and the type of person trying to enter the tunnels. Peak hours are from 8:00a to 9:59a and 4:00p to 5:59p. Faculty, and students may enter the short segments AB, BC, CD, and DA at any time. During off-peak hours upper classmen may enter the shortcuts. Faculty may enter the shortcuts at any time. People visiting the university, will be issued guest passes that will grant them access to all of the tunnels during off-peak times, but prevent them from clogging the tunnels during peak hours.

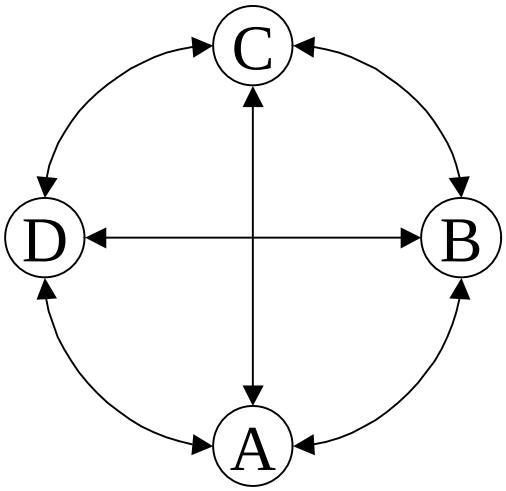
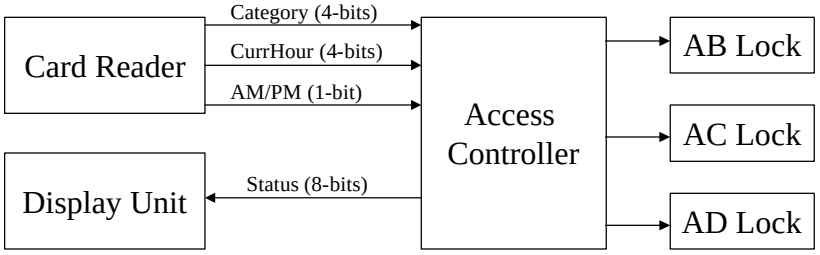


Figure 1: University Tunnel Connections

Crosswalk Signals and Entertainment Inc. have been contracted by UConn to provide access control to the underground tunnels. As a new CSE employee, you have been asked to build a portion of the circuit. Since this is your first project for CSE you will be given some guidance as you learn the tools and basics of design. It is important to think through your design options at the beginning of the project as you can save vast amounts of time building and fixing if you design carefully up front. Part of this careful design approach is preparing a test chassis to verify that your circuit functions as expected. To this end, the circuit and test unit you will build will assume that the card reader works and that the display circuitry is fully functional. If all goes well, the people working on those circuits will finish them and provide them for testing before the deadline (worth extra points if you are able to integrate successfully).

Design Overview

The system designed has a card scanner that will read an identification card and provide information about the current user. This will consist of a 4-bit word indicating the category of the user (lower division student, upper division student, faculty, guest, or no card). Also provided is the hour of day as a 4-bit word and a flag (1-bit) to indicate AM/PM. The display unit consists of 16-character by 4-line liquid crystal display (16x4 LCD). Messages will be preprogrammed into this device so that you can send an 8-bit status



word to it and it will display an intelligent message to the user. These messages have already been defined by the project lead as follows

Message	Displayed Text
0000 0000 (0x00)	Access Denied
0000 0001 (0x01)	Access Granted, Select Short Tunnel
0000 0010 (0x02)	Access Granted, Select Any Tunnel
1000 0000 (0x80)	Access Denied, Not Off-Peak Now

Considerations

This circuit is purely combinational. This means that your circuit has no concept of time and cannot remember past events. Whatever the inputs are, you should be able to determine the outputs. You will set the time of day by using a hex keypad in LogicWorks. You will also set the category of the user by using a hex keypad in LogicWorks. The AM/PM flag will be implemented as a binary switch. To make your life easier, use a pair of hex displays to show the message (don't worry about the text – we'll cover this in future projects). Also, you will need a binary probe to show the state of each of the locks that will be opened or left closed. You are free to choose the codes you want assigned for the hour, user category, and AM/PM flag provided that you use the required number of bits. By spending some time planning and drawing ideas on paper, you may find one set of codes works much better than another. Also, you may want to plan ahead for future changes that have not been specified. What needs to change in your design if we decide to grant access by student's year (Freshman, Sophomore, etc) rather than division standing? Perhaps we will add more specific error messages – if the card reader reads the card incorrectly and puts out a 4-bit code you do not recognize, what happens? Make sure you consider this in your design and document the trade offs.

Due Dates

September 3rd, 2003: Initial Design – You should have decided on all of the discrete steps necessary to build this circuit. Blocks should be identified (mostly done for you already) and codes need to be selected. Pen and paper work is fine at this stage.

September 8th, 2003: Functional Design – At this point, you should have all equations finalized and the circuit should be working in LogicWorks. Plan to show your TA a quick overview of this circuit and be asking questions if you are having difficulty with any portion of the circuit. It is recommended that you start writing a top-level description of your solution at this point as well as the objective of the project.

September 17th, 2003: Project 1 Due – The completed project along with report must be submitted as specified in the course information. Please be sure to follow the submission requirements. Remember, printed copies of your report are required along with the electronic version. A full formal report is expected, including a title page with your name, course number, section, and date. The body of the report must include a brief description of the problem you are solving (objective), a top-level design that your manager can read and understand, and a detailed description of each of the top-level blocks. For each detailed block, there should be a set of truth tables. These truth tables need to be converted to the equations actually implemented. If the equations were reduced using Boolean algebra, these steps must be shown in the report or provided in an appendix. If k-maps were used, these diagrams must be included. A copy of the circuit that is implemented from these reduced equations should follow and be referenced so the reviewing panel can understand your design. Reports must be word processed and pieced together into a single final document. Schematics can be cut and pasted in the report. If you have questions on how to do this email me or see your TA. If time permits, you will be asked to demonstrate your circuit for your TA on the due date.